REMARKS

The drawings are currently objected. Claims 1-21 are currently pending in the subject application, and are presently under consideration. Claims 1-11, 14, 15 and 18-21 are rejected. Claims 12, 13, 16, and 17 have been indicated as allowable. Claims 1, 2, 3, 6, and 15 have been amended. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I.   Drawing Objections

FIG. 2 has been objected to for failure to comply with MPEP §608.02(g) in that it does not indicate in a legend that it is prior art. Accordingly, Figure 2 has been amended by a replacement drawing submitted with this Office Action response to include an indication that it is prior art. Withdrawal of the objection to FIG. 2 is respectfully requested.

The drawings have also been objected to under 37 CFR 1.83(a) in that claimed features of the invention have been omitted from the drawing. Accordingly, new FIG. 8 has been submitted with this Office Action response, as well as corresponding additions to the Specification, as included above. It is respectfully submitted that neither the addition of FIG. 8 nor the corresponding additions to the Specification constitute new matter, in accordance with MPEP §608.01(l) and §608.04, as these additions to the drawing set and to the Specification correspond directly to the claims as originally filed (see *e.g.*, claim 10). Withdrawal of the objection to the drawings is respectfully requested.

II.   Claim Objections

Claims 1-21 are objected to because of informalities. Particularly, claims 1, 2, 3, 6, and 15 contain informalities. Accordingly, claims 1, 2, 3, 6, and 15 have been amended to correct the informalities. Withdrawal of the objection to claims 1-21 is respectfully requested.

DRAWINGS

Please amend the drawing set with the attached drawings, replacement drawing FIGs. 2 and 3 and new drawing FIG. 8, submitted with this amendment.

III.   Double Patenting

Claims 1-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-9 of U.S. Patent No. 6,781,447. Accordingly, a terminal disclaimer, in accordance with MPEP §804.02, is being submitted with this Office Action response for claims 1-9 in view of claims 1-9 of U.S. Patent No. 6,781,447. Withdrawal of the rejection of claims 1-9 is respectfully requested.

Claims 10-11, 14-15, and 18-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18-19, 23-24, and 27-28 of copending Application No. 10/004,581. Accordingly, a terminal disclaimer, in accordance with MPEP §804.02, is being submitted with this Office Action response for claims 10-11, 14-15, and 18-19 in view of claims 10-11, 14-15, and 18-19 of copending Application No. 2003/0103582. Withdrawal of the provisional rejection of claims 10-11, 14-15, and 18-19 is respectfully requested.

IV.   Rejection of Claims 20 and 21 Under 35 U.S.C. §102(e)

Claims 20 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,236,687 to Caso et al. ("Caso"), admitted prior art by Applicant. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 20 recites a phase locked loop comprising a block decoder which decodes phase stabilized observables at a decode rate to generate decoded data and an estimate of a phase error of an input modulated signal by derotation of the series of phase stabilized observables based on decoded data and updates the phase error at each codeword. Caso discloses an improved digital decision directed phase locked loop (DD-PLL) for use with short block codes using phase shift keying modulation (Abstract). However, Caso does not disclose that a block decoder generates an estimate of a phase error of the input modulation signal by derotation of a series of phase stabilized observables based on decoded data and updates phase error at each codeword, as recited in claim 20. Instead, Caso discloses that a vector error evaluator (FIG. 3, Reference No. 319) evaluates a set of vector pairs of phase stabilized observables in accordance with decoded

data at each codeword to generate a decision directed phase error estimate which is filtered by a digital filter to yield an update of an estimated phase at every codeword (col. 8, ll. 38-43). Therefore, the phase error estimate, as disclosed by Caso, is not generated by a block decoder, as recited in claim 20, but is instead generated by a vector error evaluator within the phase locked loop that is a separate device than a block decoder.

For the reasons described above, claims 20 and 21 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

Date _1/18/05_

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